

Tech Talk

Fine Lines in High Yield (Part CLIII)

Full-Build Electroless Copper

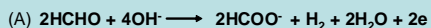
Karl H. Dietz (for CircuiTree Magazine, June, 2008)



Karl Dietz is the manager at DuPont's Electronic Materials Laboratory, Research Triangle Park, NC. His responsibilities include application studies for printed circuit materials. Karl has 35 years of experience in a variety of R&D, manufacturing and quality control functions and holds a PhD. in organic chemistry from the University of Frankfurt, Germany. If you would like to participate in the exchange or if you have any questions, Karl Dietz can be reached at 919-248-5248, fax: (919) 248-5132, or via e-mail <Karl.h.dietz@usa.dupont.com>.

Electroless copper plating is widely used in PWB fabrication to form a metal seed layer on through-hole and blind via hole walls to enable the formation of a thicker copper deposit by electroplating. The use of electroless copper plating to deposit all of the copper ("full-build") made some inroads in the 1980's but disappeared later almost completely for a number of reasons we shall take a look at. It is conceivable that full-build electroless copper may stage a comeback due to the fact that novel patterning processes can eliminate some of the drawbacks of the original full-build electroless process.

The electroless copper process requires a source of copper ions, a reducing agent, typically formaldehyde, and a catalyst that initiates the reaction. Formaldehyde is oxidized to formic acid in the presence of strong alkali, generating two electrons that reduce cupric ions to metallic copper (see equations of Figure 1).



To prevent the formation of copper hydroxide precipitate, copper ions are complexed with a complexing agent such as EDTA (ethylenediamine tetraacetic acid), THPED (tetrakis-(2-hydroxypropyl)-ethylenediamine) or a variety of alpha-hydroxy-carboxylic acids. The bath is stabilized by cyanide, substituted quinoline sulfonic acids (Ref. 1), 2-mercaptobenzothiazole or a variety of other stabilizers. The bath composition can be automatically controlled. Formaldehyde is titrated with bisulfate, the copper concentration is measured colorimetrically, the pH is measured with a pH probe, and the cyanide concentration is checked with an ion-selective electrode (Ref. 2).

The classic full-build electroless copper process, pioneered by the Kollmorgen Corpo-


ration and licensed to a number of companies, including Hitachi and IBM, provides the palladium catalyst embedded in the dielectric base material. After drilling the through-holes, a photoresist is laminated to the surface, is exposed and developed. Standard aqueous processable dry film photoresists cannot be used in this process because they don't survive the long exposure to the strong alkali of the electroless copper bath. Therefore, solvent processable resists were used that developed in trichloroethane (methylchloroform) and stayed with the board as a permanent coating. The board was then treated with chromic/sulfuric acid to promote adhesion of the electroless copper to the dielectric surface, hydrofluoric acid was then employed for glass fiber etch-back in applications that required such a step; then followed the full-build electroless copper process. Another truly additive process uses a different catalyst to initiate the electroless copper deposition. The dielectric base material contains a copper salt or copper oxide. After resist lamination, exposure and development, the copper oxide at the surface of the dielectric in the developed areas is reduced to metallic copper which acts as a catalyst for the electroless copper process.

By 1986, the full-build electroless process had captured only 2% of the North American PWB market (Ref. 3) while it had found much greater acceptance in Japan in the low-cost consumer electronics market. The drawbacks of the full-build electroless process can be summarized as follows:

- The need for an alkaline-resistant solvent processable photoresist. When solvent resists gave way to aqueous processable resists, due to environmental and health concerns, it became difficult to find suitable photoresists for the full-build electroless copper process.
- PWB fabricators preferred to be able to use a variety of base materials to serve a broad customer base which was not



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possible with the specialty laminate required for the full-build process.

- The full-build process involved pretty nasty wet chemistry such as chromic acid and hydrofluoric acid.
- Compared to electroplating, the full-build electroless copper process is very slow.
- Waste treatment of the electroless bath is more involved than maintaining an acid copper electroplating bath.
- Early versions of this process yielded copper deposits with poor ductility, leading to corner cracks.
- There was concern about problems with insulation resistance and ionic contamination due to the catalyst in the dielectric, especially with very fine circuits.
- Last not least, there was the lack of a military standard that could have promoted the acceptance of the technology

Having said this, one should mention the considerable advantages of the full-build electroless process:

- The copper deposit is of more uniform thickness than electroplated copper because there are no primary and secondary current density distributions that lead to uneven copper thicknesses.
- The copper deposit in high aspect ratio plated through-holes is very uniform because there are no throwing power problems that lead to dog-bone shaped copper thickness variation which has been a problem with copper electroplating. Taking advantage of this good through-hole plating performance of electroless copper, Hitachi was able to build multilayer boards with more than forty layers and very high aspect ratio plated through-holes.
- There is no etching step and the resulting waste stream from this process step.

It should also be mentioned that the initial problems with corner cracking was overcome with improved bath formulations. Although electroless copper never achieved the elongation and ductility of electroplated deposits, Karl Minten and others (Ref. 4) have shown that improved full-build electroless baths, those with improved elongation as well as those with higher tensile strength, pass the customary reliability tests. In addition, the deposition rate of these baths is much improved.

There are several variations of the full-build process. Here is a short overview.

One interesting variation is **Hitachi's TAF-2 process** which starts with copper-clad laminate and requires a standard, full etch step. One might call it a "semi-additive" process but this could lead to confusion since this term is exclusively used for the process that starts with bare dielectric, employs a thin electroless copper deposit, followed by structuring a plating resist, pattern plating, stripping, and removal of the thin seed layer by a differential etch step. The TAF-2 on the other hand, starts with copper-clad laminate, the laminate is drilled, a catalyst is deposited, an etch resist is laminated, exposed, and developed, followed by etching and resist stripping. Now a second resist that can

hold up in the electroless copper chemistry is laminated over the circuitized surface, is exposed and developed to open up the catalyzed through-holes. Now follows the full-build electroless copper deposition in the through-holes (sometimes referred to as "button plating process") after which the photoresist is stripped.

In the late 1980s, **Ibiden** introduced the **AAP/10 Process** (Ref. 5), a development that extended the technology of a similar process developed by Hitachi, called AP-II. The Ibiden process starts with a dielectric substrate onto which a heat-resistant adhesive is coated. The board is then drilled, the hole-wall is roughened, and a catalyst is applied to the entire surface and hole-walls. A dry film, capable of surviving the full-build electroless process is then structured for full-build pattern plating. The dry film may be left as a permanent resist or may be peeled off.

A process was patented by **IBM** (European Patent Application No. 85114052.5) that creates a palladium catalyst pattern from a palladium compound in the vapor phase. The dielectric substrate surface is covered with a photoresist or polymer that is irradiated through a mask by an excimer laser. The polymer is removed by the irradiation during this process in the irradiated areas and the exposure causes a reduction of the palladium compound and deposition of metallic palladium in the areas where the polymer has been removed. Circuits are then formed in these areas by a full-build electroless copper process.

Sawyer (U.S. Pat. No. 4,388,351) describes a fully additive process where photoresist is patterned on the surface of a dielectric base material. The dielectric surface in the resist-free areas is then chemically roughened. A catalyst capable of initiating the electroless copper process is then deposited on the entire surface, both resist and dielectric. A thin electroless copper layer is then formed on the surface. The resist, covered with catalyst and thin electroless copper is then lifted off, leaving a copper seed layer pattern which is then build-up with full-build electroless copper. The disadvantage of this process is the fact that the photoresist has to be a solvent processable resist in order to survive the short electroless copper deposition before it is removed. The AT&T process follows the Sawyer's processing sequence, except it is able to use aqueous processable photoresists.

The process by **John Dorey** et al (US Pat. No. 4,574,031, assigned to AT&T) starts with a dielectric substrate that is covered with an aqueous processable photoresist which is exposed and developed. The dielectric at the bottom of the developed resist channels is subjected to a swell and (chromic acid) etch treatment to create a porous surface. This surface is then catalyzed and a flash deposit of copper from an hypophosphite electroless copper bath (pH=9) is formed. The photoresist, and any unwanted copper deposit on its surface are then lifted off and the copper seed layer is built up in a full build electroless copper bath.

One way to avoid the use of solvent processable resist in the full-build electroless process is to run a panel plate/ tent & etch processing sequence, as suggested in Reference 3. The drilled multilayer board, ideally with thin outerlayer copper, is processed through full-build electroless copper to deposit the desired through-hole copper thickness. An aqueous processable dry film photoresist can then be used in the tent & etch process.

In recent years, new processes make use of full-build electroless copper without the need for a solvent resist. **LPKF** has introduced a process that uses dielectric resins that contain a copper salt. A laser exposes the dielectric surface in a pattern whereby the copper salt is

converted to copper in the exposed areas. This can be done on 3D-surfaces. The catalyzed areas are then built-up with electroless copper.

LPKF's LDP (laser direct patterning, Ref. 6) process also avoids the use of solvent resist by defining a metal pattern by laser ablation. A thin metal layer is selectively ablated from a metal-clad dielectric (e.g. for RFID tags) by an excimer laser working at 248nm or 308nm, using a chrome on quartz photomask. The metal layer thickness can be up to 150 nanometers. The ablation threshold for single shot ablation is 50-500 mJ/sqcm, depending on the polymer. The metal pattern can then be built up (e.g. to 12.5 micron) by electroless copper plating. The smallest feature size after laser ablation is 15 micron. After electroless plating, the width of the copper traces widens to 20 micron since there is no resist channel that defines the width of the trace.

For completeness sake one should also mention a fully additive process which is not based on full-build electroless copper, namely the **Michaelson Process** (US Patent 4,581,301, April 8, 1986). Mr. Michaelson pre-drills a dielectric substrate, screen prints a seed layer pattern on both surfaces and onto the hole walls. The seed layer is carbon in an epoxy matrix. Then one side of the board is brought in close contact with the cathode surface in a copper electroplating bath. The seed layer pattern on the non-covered side receives current through the many holes from the backside of the board as copper is plated up. This is then repeated on the other board surface. I don't know if this was ever practiced on an industrial scale.

Acknowledgment

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